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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,133	07/15/2003	Duy-Phach Vu	0717.1063-007	7858

21005 7590 09/14/2004

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EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,133	VU ET AL.	
	Examiner	Art Unit	
	Kenneth A Parker	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/15/2003
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-2 and 4-6 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2-7 of U.S. Patent No. 6593978. Although the conflicting claims are not identical, they are not patentably

distinct from each other because the current claims are broader than those of the patent. See claims of patent an application below:

Application:

1. A method of fabricating an active matrix display comprising:

forming a silicon layer over an insulating layer and a supporting substrate

forming an array of transistors with the silicon layer to form an active matrix circuit on the supporting substrate;

forming an array of pixel electrodes with a polycrystalline silicon material; and

transferring the array of transistors and the array of pixel electrodes to a second substrate.

2. The method of Claim 1 further comprising forming interconnects between the transistors and the pixel electrodes.

4. The method of Claim 1 wherein the second substrate comprises an optically-transmissive substrate.

5. The method of Claim 4 further comprising positioning a material between the array of pixel electrodes and a counter electrode, such that selective actuation of a pixel electrode produces an electric field across a portion of the material disposed between the pixel electrode and the counter electrode, thereby producing a change in a light transmission property of the material. (inherent to the use with a liquid crystal material therein).

Patent claims:

1. A method of fabricating an active matrix liquid crystal display comprising:

forming a silicon layer over an insulating layer and a supporting substrate;

forming an array of transistors with the silicon layer to form an active matrix display circuit on the substrate; forming an array of pixel electrodes with a polycrystalline silicon material;

transferring the array of transistors and the array of pixel electrodes to an optically transmissive substrate; and positioning a liquid crystal material between the array of pixel electrodes and a counter electrode to form an active matrix liquid crystal display.

2. The method of claim 1 further comprising forming interconnects between each pixel electrode and a transistor circuit.

3. The method of claim 1 wherein each transistor comprises a source, a drain, a channel and a gate over the channel.

4. The method of claim 1 further comprising transferring the array of transistors and the array of pixel electrodes from the supporting substrate to a transfer substrate.

5. The method of claim 1 wherein the transistors comprise a single crystal silicon material.

6. The method of claim 4 wherein the transferring step further comprises bonding the silicon layer to the transfer substrate.

7. The method of claim 6 further comprising bonding with an adhesive material.

19. A method of fabricating a plurality of active matrix liquid crystal displays comprising:

forming a single crystal silicon layer over a supporting substrate; forming a plurality of arrays of transistors with the silicon layer to form a plurality of active matrix display circuits on the substrate;

forming an array of pixel electrodes for each array of transistors, wherein the pixel electrodes comprise a polycrystalline silicon material;

positioning a liquid crystal material between each array of pixel electrodes and a counterelectrode; and separating regions of the silicon layer to form a plurality of displays.

Claim 3 is are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2-7 of U.S. Patent No. 6593978 in view of EP545694. Although the conflicting claims are not identical, they are not patentably distinct from each other because the missing element was a light shield betweent the transistor and the second substrate, and the use of an interposing shield was taught in EP0545694, which had the advantage that it shield the transistor from light. Therefore, it would have been obvious to one of ordinary skill to employ a light shield as taught by EP0545684 for the advantage of shielding the transistor from light.

Claims 1-2 and 4-6 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 16-18 of U.S. Patent No. 5757445. Although the conflicting claims are not identical, they are not

patentably distinct from each other because the current claims are broader than those of the patent- see below.

Application claims :

1. A method of fabricating an active matrix display comprising:

forming a silicon layer over an insulating layer and a supporting substrate

forming an array of transistors with the silicon layer to form an active matrix circuit on the supporting substrate;

forming an array of pixel electrodes with a polycrystalline silicon material; and

transferring the array of transistors and the array of pixel electrodes to a second substrate.

2. The method of Claim 1 further comprising forming interconnects between the transistors and the pixel electrodes.

4. The method of Claim 1 wherein the second substrate comprises an optically-transmissive substrate.

5. The method of Claim 4 further comprising positioning a material between the array of pixel electrodes and a counter electrode, such that selective actuation of a pixel electrode produces an electric field across a portion of the material disposed between the pixel electrode and the counter electrode, thereby producing a change in a light transmission property of the material. (inherent to the use with a liquid crystal material therein).

Patent claims:

16. A method of fabricating an active matrix liquid crystal display comprising:

forming a silicon layer over an insulating layer and a supporting substrate;

forming an array of transistors with the silicon layer to form an active matrix display circuit;

forming an array of pixel electrodes with a polycrystalline silicon material;

bonding the array of transistors onto an optically transmissive substrate with a bonding layer;

removing the supporting substrate from the display circuit; and

positioning a liquid crystal material between the array of pixel electrodes conductively connected to the active matrix display circuit and a counterelectrode element.

17. The method of claim 16 wherein the removing step further comprises chemically etching the supporting substrate to release the active matrix display circuit.

18. The method of claim 16 further comprising forming interconnects between each pixel electrode and a transistor circuit.

Claim 3 is are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2-7 of U.S. Patent No. 5757445 in

view of EP545694 Although the conflicting claims are not identical, they are not patentably distinct from each other because the use of an interposing shield was taught in EP0545694, which had the advantage that it shield the transistor from light. Therefore, it would have been obvious to one of ordinary skill to employ a light shield as taught by EP0545684 for the advantage of shielding the transistor from light.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth A Parker
Primary Examiner
Art Unit 2871